Bi-weekly Status Report 2
Senior Design, December 2020, Team 14

Introduction of Real-World Signals and Systems into ECpE DSP Laboratory Curriculum

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Progress Summary:

Over the last two weeks, we have been focused on coordinating with faculty regarding lab implementation priorities. We were involved with ETG's formal presentation of the CyDAQ platform as it transitions fully to a senior design effort. We then held a second meeting with Signals and Systems faculty to discuss lab development and implementation strategies for this semester's EE224 lab. We also saw the first use of CyDAQ in a teaching lab, when EE423 students evaluated and characterized preset filters with the hardware functioning as a black box.

Individual Contributions by Team Member:

- **Brady Anderson (Biweekly: 12; Cumulative: 24)**
  - Debugged FPGA firmware, fixed Vivado workspace migration errors
    - Deployed firmware onto the Zynq to verify that the firmware is functional
  - Attended ETG presentation to DSP faculty explaining the CyDAQ and its possible uses in signal processing courses like EE224, EE324, EE321, etc.
  - Met with DSP professors to discuss integration of the CyDAQ into this semester's EE224 labs
  - Reinstalled Python 3 to enable front-end testing
    - Connected the Python front-end to the Zynq, verified that commands can be sent to the FPGA
- **Sam Burnett (Bi-weekly: 13, Cumulative: 25)**
  - Developed signal flow theory of implementation for pulse width modulation lab.
  - Presented to Cydaq overview to faculty and department chair
    - PMIC Design principles and specifications
    - Audio frequency lab ideas and concepts
    - Communication systems lab ideas and concepts
  - Met a second time with faculty members to discuss curriculum improvements and upcoming lab development priorities and timeline.
  - Prototyped XADC direct input passive level shifter/attenuator
  - Supported 'black box' implementation of preset filters for evaluation by EE423 students in lab with Dr. Kim and ETG
- **Mitchell Hoppe (Weekly: 12.5; Cumulative: 24.5)**
  - **https://github.com/alejandroautalan/pygubu**
  - Worked on improving the stability and usability of the python front end.
  - Updated the website repo with team names, bios, and photos.

- Configured git repos with initial commits and necessary branches
- Had meetings with faculty about the use of CyDaq in the labs.
    - Presented CyDAQ to EE faculty to propose its use in EE 224 and 324 labs.
    - Met with Julie and Bolstad to discuss the use of CyDAQ in the lab and what changes to make for the upcoming labs.

- **Max Kiley (Biweekly: 12; Cumulative: 24)**
    - Git familiarization
    - Familiarization with Trello
    - Worked on testing the filters on multiple CyDAQ boards.
    - Continued soldering various through-hole components on multiple CyDAQ boards
    - Finished assembling multiple CyDAQ into cases.

- **Emily Lagrant (Biweekly: 13; Cumulative: 25)**
    - Attended weekly planning meetings to discuss activities and plans with faculty advisor
    - Sat in on meeting for ETG and various faculty members to discuss the CyDAQ board.
    - Met with 224 professors to discuss what each party wanted to see in different labs and started planning 4 labs that need to be done before Spring Break
        - Labs Include:
            - CyDaq basics, signal acquisition, time and frequency analysis
            - Digital Filtering of a Noisy Signal
            - Aliasing
            - 2 week project; heart beat lab, lie detector, fitness tracker
    - Started working with past 224 labs to test which labs are meeting learning objectives
    - Set up Trello tasks and organized task board

- **Isaac Rex (Bi-Weekly: $\int_0^3 \frac{2}{3}t^3 + \frac{1}{3}dt + \cos(\frac{3\pi}{\beta}),\ \beta = 3$; Cumulative: 25.5)**
    - Presented CyDAQ hardware and initial lab concepts to major signals faculty
        - Obtained feedback from staff and helped guide direction
    - Met with Dr. Dickerson and Dr. Bolstad about implementing labs this Spring
        - Started planning labs and working toward learning objectives
    - Organized all hardware design files on hardware Git repository
    - Updated CyDAQ mechanical BOM to include all enclosure parts
    - Contacted professors for EE224 and EE324 to obtain current labs
        - EE224 labs pushed to our Labs Git repository
        - Waiting for Dr. Tabassum to provide EE324 labs
    - Started obtaining initial data for particular EE224 labs

    - Found design references for planned controls lab
        - Began mathematical model based on references and lab design

Pending Issues:

- No set standard for documenting lab ideas.
- Vivado is not consistent about relative and absolute paths, which may make design portability difficult.

Plans:

- Isaac:
    - Begin Introduction To CyDAQ Lab, to be completed by 3/20
        - Finished draft by 3/5
    - Continue researching controls lab design, initial system model to be completed by 2/19
    - Obtain and push to Git current EE324 labs, to be completed by 3/1
    - Prototype signal analysis for EE224/CprE288 tie-in, to be completed by 3/15
        - Send Dr. Dickerson signal analytics by 3/1
- Emily: Begin writing some labs
- Brady:
    - Commit latest firmware to Git and make sure paths will not be an issue (or will be an issue that can be dealt with)
    - Obtain CyDAQ board from ETG and start testing full system operation
    - Investigate FreeRTOS and consider implementation strategies
- Sam:
    - Implement PWM design block and test signal theory in lab environment for PWM intuition
    - Test XADC passive level shifter/attenuator
    - Write prelab and lab document for PWM intuition